IN THE CLAIMS

Claim 1 (Currently Amended): A semiconductor device comprising:

a first interconnect layer arranged above a surface of a substrate on which a functional semiconductor region is formed;

an inter layer dielectric covering a surface of said first interconnect layer;

a second dielectric layer which is coated on a surface of said inter layer dielectric so as to embed a concave portion of an upper surface thereof;

a silicon nitride film formed so as to cover entirely a top surface of said inter layer dielectric;

a metal interconnect layer covering said silicon nitride film, said metal interconnect layer being consisted of gold material; and

a planarized polyimide which is formed directly on a surface of the silicon nitride film and directly surrounding the metal interconnect layer including a side wall thereof,

wherein a portion of the ~~polyimide resin layer~~ planarized polyimide is removed at a part of a region of the metal interconnect layer and a bonding wire is connected to the region of the metal interconnect layer.

Claim 2 (Canceled).

Claim 3 (Previously Presented): A semiconductor device according to claim 1, wherein said silicon nitride film is formed by high-density plasma CVD method.

Claim 4 (Canceled).

Claim 5 (Withdrawn): A method for manufacturing a semiconductor device comprising steps of:

a process for forming a foundation interconnect layer on a surface of a semiconductor substrate on which a functional semiconductor region is formed;

a process for forming an inter layer dielectric on said foundation interconnect layer of which surface is shaped as convex and concave shape;

a process for forming silicon nitride film on said inter layer dielectric;

a process for forming metal interconnect layer as an uppermost layer interconnectas an upper layer of said silicon nitride film, said metal interconnect layer being consisted of gold; and

a process for coating a polyimide resin film on said metal interconnect layer and planarizing surface thereof.

Claim 6 (Withdrawn): A method for manufacturing a semiconductor device according to claim 5, wherein said metal interconnect layer is connected to said foundation interconnect layer through a though hole formed in-between thereof and further wherein said interconnect layer is low in resistance and formed thicker than thickness of said foundation interconnect layer.

Claim 7 (Withdrawn): A method for manufacturing a semiconductor device according to claim 6, wherein said method further includes a process for removing a part of region of said polyimide resin layer, and a process for wire-bonding at said part of region so as to connect to a surface of said metal interconnect layer.

Claim 8 (Currently Amended): A semiconductor device comprising:

a first interconnect layer covering a first portion of a surface of a functional semiconductor region;

an inter layer dielectric covering a second portion of the surface of the functional semiconductor region and a portion of a surface of said first interconnect layer, thereby forming a contacting hole on the surface of the first interconnect layer;

a second dielectric layer which is coated on a surface of said inter layer dielectric so as to embed a concave portion of an upper surface thereof;

a silicon nitride film covering an entire top surface of said inter layer dielectric around the contacting hole on the surface of the first interconnect layer;

a barrier layer covering the contacting hole and a portion of a surface of the silicon nitride film around the contacting hole, thereby forming a barrier layer region;

a metal interconnect layer consisting of gold material covering the barrier layer region, thereby forming a metal interconnect region; and

a planarized polyimide which is formed directly on a surface of the silicon nitride film and directly surrounding the metal interconnect layer including a side wall thereof,

wherein a portion of the ~~polyimide resin layer~~ planarized polyimide is removed at a part of a region of the metal interconnect layer and a bonding wire is connected to the region of the metal interconnect layer.

Claim 9 (Previously Presented): The semiconductor device of claim 8, wherein the barrier layer consists of titanium.

Claim 10 (Previously Presented): The semiconductor device of claim 9, wherein the first interconnect layer consists of aluminum.

Claim 11 (Previously Presented): The semiconductor device of claim 8, wherein the first interconnect layer consists of aluminum.

Claim 12 (Previously Presented): The semiconductor device of claim 8, wherein the inter layer dielectric consists of USG film.

Claim 13 (Currently Amended): The semiconductor device of claim 8, wherein the functional semiconductor region further comprises a polysilicon gate isolated from the first interconnect layer by a ~~second~~ third dielectric layer, wherein the first interconnect layer is connected to the polysilicon gate through a contacting area disposed within the ~~second~~ third dielectric layer.

Summary of the Office Action

Claims 1, 3, 8 and 10-12 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable by Loboda et al. (US, 5,818,071), in view of Braeckelmann et al. (US, 6,218,302).

Claim 9 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Loboda et al. in view of Toyosawa et al. (US, 6,441,467).

Claims 1 and 8 stand rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite.

Summary of the Response to the Office Action

Claims 1, 8, and 13 are amended to further define the invention. Claims 5-7 are previously withdrawn from consideration and claims 2 and 4 are previously cancelled without prejudice or disclaimer. Accordingly, claims 1, 3, and 8-13 are presently pending for consideration.

Rejection of claims under 35 U.S.C. § 112, second paragraph

Claims 1 and 8 stand rejected under 35 U.S.C. §112, second paragraph, as allegedly indefinite. Applicants respectfully submit that the informalities noted by the Office Action do not rise to the level of indefiniteness. However, Applicants have amended claims 1 and 8 in accordance with the comments of the Examiner. Applicants respectfully submit that the amendments do not narrow the intended scope of the claims and therefore do not intend to relinquish any subject matter by these amendments. Accordingly, Applicants respectfully assert that the rejection of claims 1 and 8 under 35 U.S.C. §112, second paragraph, should be withdrawn.

All Claims Define Allowable Subject Matter

Claims 1, 3, 8 and 10-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable by Loboda et al., in view of Braeckelmann et al. And, claim 9 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Loboda et al. in view of Toyosawa et al. Applicants respectfully traverse the rejections for at least the following reasons.

With respect to independent claims 1 and 8, as amended, Applicants respectfully assert that Loboda et al. and Braeckelmann et al., whether taken singly or combined, does not teach or suggest at least a feature including "a second dielectric layer which is coated on a surface of said inter layer dielectric so as to embed a concave portion of an upper surface thereof." On page 3 of the Action, the Office alleges that "FIG. 1 of Loboda et al. shows most aspect of the instant invention except an inter layer dielectric and the polyimide layer is removed at a part of a region of the metal interconnect layer and a bond wire is connected to the region of the metal interconnect layer. FIG. 11 of Braeckelmann et al. shows that an inter layer dielectrid (22) and a silicon nitride film (23) formed so as to cover entirely a top surface of said interlayer dielectric, covering over said silicon nitride film covering a surface of the first interconnect layer and the polyimide layer is removed at a portion of a region of the metal interconnect layer and a bond wire (1104) is connected to the region of the metal interconnect layer." As a result, the Office alleges that "it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Loboda et al. to the device of Braeckelmann et al. in order to have an additional inter layer dielectric layer under the silicon nitride layer for structural strength and the polyimide layer removed at a part of a region of the metal interconnect layer for wire connection." Applicants respectfully disagree.

In contrast to the Applicants' claimed invention, Loboda et al. teaches the use of silicon carbide as a barrier layer to prevent the diffusion of metal atoms between adjacent conductors separated by a dielectric material (Loboda et al., Abstract). Braeckelmann et al. teaches a formation of interconnect over a substrate such that an adhesion/barrier layer (81), a seed layer (82), a conductive film (83), and a copper-alloy capping film (84) are deposited over the substrate (10) to form an interconnect (92) (Abstract, Braeckelmann et al.). However, Applicants respectfully submit that neither Loboda et al. nor Braeckelmann et al., teach or suggest the formation of SOG layer with organic dielectric (organic SOG layer), which is the element that best matches to a "interlayer dielectric" as claimed, underneath the silicon nitride film. In addition, Loboda et al. and Braeckelmann et al. are both silent about the organic SOG layer embeds the concave portion of the USG layer (i.e., inter layer dielectric) positioned at an upper side, as recited in independent claims 1 and 8, as amended, as well as, discussed on page 8, lines 20-25 of the original specification.

Accordingly, Applicants respectfully assert that Loboda et al. and Braeckelmann et al., whether taken singly or combined, does not teach or suggest every element recited in at least the amended independent claims 1 and 8. In addition, Applicants respectfully assert that Toyosawa et al. fails to cure the deficiencies of Loboda et al. Thus, in light of the arguments presented above, Applicants respectfully request that rejection of claims under 35 U.S.C. § 103(a) be withdrawn since none of cited prior art, whether taken singly or in combination, teach or suggest at least the features of amended independent claims 1 and 8, hence dependent claims 3, 9-13. Furthermore, Applicants respectfully submit that dependent claims 3 and 9-13 are allowable for all of the reasons discussed above with regard to amended independent claims 1 and 8, from

which they respectfully depend, as well as the individual features that dependent claims 3 and 9-13 recite.

CONCLUSION

Applicants respectfully request that this Amendment under 37 C.F.R. § 1.116 be entered by the Examiner, placing all pending claims in condition for allowance. Applicants submit that the claim amendments do not raise new issues or necessitate additional search of the art by the Examiner.

Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact Applicants' undersigned representative to expedite the prosecution. If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted

MORGAN, LEWIS & BOCKIUS LLP

By: _____
Sumiyo Onda
Reg. No. L0289

Dated: September 20, 2006

CUSTOMER NO. 009629
MORGAN, LEWIS & BOCKIUS LLP
1111 Pennsylvania Avenue, N.W.
Washington, D.C. 20004
Telephone: (202) 739-3000
Facsimile: (202) 739-3001